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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,915	LU ET AL.	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 14 objected to because of the following informalities: use of "copies" between "code to be" and "from the I/O." Examiner reads "copies" as "copied." Appropriate correction is required.

Claim 15 objected to because of the following informalities: "each node further comprises at least one copy of the BIOS code the CPU firmware" where the objection lies within "BIOS code the CPU." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9 and 16 rejected under 35 U.S.C. 102(e) as being anticipated by Gentile (U.S. PGPub 2002/0147941 A1).

As in claim 9, Gentile discloses a first node that includes a first set of one or more central processing units (CPUs) ("computer system" of Fig. 2 #22, paragraph [0010] lines 1-2, paragraph [0011] line 6);

a second node communicatively connected to the first node, wherein the second node includes a second set of one or more CPUs ("BIOS recovery server" of Fig. 2 #21, 23, or 24, paragraph [0012] lines 1-2, paragraph [0013] lines 1-4, where it is inherent that a "server" has a central unit for processing information (CPU));

a first firmware unit in the first node, communicatively connected to the first set of one or more CPUs (paragraph [0011] lines 4-7);

BIOS code in the first firmware unit (paragraph [0010] lines 2, 5-9);

a second firmware unit in the second node that also contains the BIOS code, the second firmware unit communicatively connected to the second set of one or more CPUs (paragraph [0013] lines 4-5, paragraph [0006] lines 9-14 where it is inherent for "firmware" to be present in the second "BIOS recovery server" node in order to store and retrieve "utilities" and communicate between itself and the first "computer system" node);

and BIOS recovery logic, in at least one of the first and second firmware units, that automatically recovers from BIOS corruption by causing a copy of the BIOS code from the second firmware unit in the second node to be copied to the

first firmware unit the first node, in response to detecting corruption in the BIOS code in the first node (Fig. 1, paragraph [0012] lines 1-5, paragraph [0013] lines 1-7, where it is inherent that "computer system" downloads a copy of the uncorrupted BIOS from the "BIOS recovery server").

As in claim 16, Gentile discloses a program product that provides automatic basic input/output system (BIOS) recovery in a multi-node computer system (MCS) with first and second nodes, a first firmware unit in the first node, and a second firmware unit in the second node, the program product comprising:

a computer-usable medium encoding recovery instructions which, when executed, perform operations comprising: in response to initiation of a boot sequence for the MCS, automatically checking a BIOS image in the first firmware unit in the first node of the MCS for corruption (Gentile, Fig. 1, paragraph [0010] 4-11, where calculating a checksum [or any other method for determination of corrupt BIOS code] implies use of a program product);

and in response to detecting corruption of the BIOS image in the first firmware unit, automatically recovering from the corruption of the BIOS image by causing a good BIOS image from the second firmware unit in the second node to be copied to the first firmware unit in the first node (Gentile, Fig. 1, paragraph [0006] and paragraph [0013]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7,10-15, 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Gentile (U.S. PGPub 2002/0147941 A1) in view of Applicant's admitted prior art (hereinafter "AAPA").

As in claim 1, Gentile discloses a method of recovering a corrupt BIOS in an information handling system, wherein an automatic BIOS image check in a first node is automatically recovered by copying a good BIOS image in a second node to corrupt BIOS image in the first node, if first node BIOS is found to be corrupt. Gentile's information handling system consists of a first firmware unit ("computer system" depicted in Fig. 2 and described in paragraph [0010]) with an automatic checking of a BIOS image ("validity check" depicted in Fig. 1 and described in paragraph [0010]). Gentile further discloses a second firmware unit ("BIOS recovery server" depicted in Fig. 2 and described in paragraph [0013]) that copies its good BIOS image to the first firmware unit for BIOS recovery (Fig. 1 #18, 19 and 20, and described in paragraph [0013]. Examiner reads "computer

system then downloads the BIOS image" as the copying from second to first firmware units.). However, Gentile does not teach automated recovery of BIOS in a "multi-node computer." AAPA discloses that information handling by "network systems," including implementation of a BIOS, can be done in a "multi-node computer" (see pages 2 and 3 of the AAPA specification).

It would have been obvious to a person skilled in the art at the time the invention was made to implement the BIOS recovery within a network environment as disclosed by Gentile in a similar "information handling system" such as a "multi-node computer." This would have been obvious because a person skilled in the art would have understood that the "multi-node computer" is a scaled down version of a "networking system" as was taught by AAPA with a similar plurality of firmware units, internodal connections, multi-nodal switch devices, and overall functionality, and therefore use of a BIOS recovery system would have been appropriate for such described systems regardless of physical size.

As in claim 2, AAPA and Gentile disclose the multi-node computer comprises multiple nodes, with each node containing a copy of the BIOS image (AAPA specification, page 2 line 29 through page 3 line 2. Gentile discloses a "computer system" and a "BIOS recovery server," each containing a copy of the BIOS image: "computer system" BIOS image: Fig. 1 #11; paragraph [0010] lines 7-9; "BIOS recovery system" BIOS image: Fig. 1 #19; paragraph [0013] lines 4-5);

determining if any of the nodes contain a good copy of the BIOS image (Gentile's validity check" depicted in Fig. 1 and described in paragraph [0010]);

and in response to determining that at least one node contains the good copy of the BIOS image, automatically copying the good copy of the BIOS image to any nodes that contain a corrupted copy of the BIOS image (Gentile, Fig. 1 #18, 19 and 20, and described in paragraph [0013]).

As per claim 3, AAPA and Gentile disclose the first node includes a first central processing unit (CPU) hub, the second node includes a second CPU hub, and the multi-node computer further comprises a multi-port switch for internodal communications (AAPA specification, page 3 lines 1-6);

the method further comprises configuring the multi-port switch to provide a communication path between the first CPU hub and the second CPU hub (AAPA, page 3 lines 6-10);

and the operation of automatically recovering from the corruption of the BIOS image comprises copying the good BIOS image from the second node to the first node via the multi-port switch (Gentile, Fig. 1 #18, 19 and 20, and described in paragraph [0013]).

As in claim 4, AAPA and Gentile disclose the first firmware unit comprises a central processing unit (CPU) firmware unit (AAPA specification, page 3 lines 2-4; Gentile, paragraph [0011] lines 5-6);

the multi-node computer also includes an input/output (I/O) firmware unit (AAPA specification, page 3 lines 2-4; Gentile, paragraph [0010] lines 7-9, by nature of the Basic Input/Output System, any combination of hardware and software specifically relating to the storage and functionality of the BIOS would be considered as "I/O firmware.");

in response to detecting corruption of the BIOS images in the CPU firmware unit, automatically copying a good BIOS image from the I/O firmware unit to the CPU firmware unit (Gentile, paragraph [0011] lines 3-5 disclose detection of corrupt BIOS; paragraph [0013] lines 4-7 disclose automatic programming into the "I/O firmware" into the "CPU firmware unit" upon system reboot, where one skilled in the art would understand that BIOS code gets "programmed" into "CPU firmware" upon initialization of the system itself.).

As in claim 5, Gentile and AAPA disclose the first node includes a first CPU hub, the second node includes a second CPU hub, and the multi-node computer further comprises a multi-port switch for internodal communications communicatively interposed between the first CPU hub and the I/O firmware unit (AAPA: specification, page 3 lines 3-9 (Fig. 1); *EE TIMES* paragraph 7; *The Register* paragraph 6);

and the operation of automatically recovering from the corruption of the BIOS image comprises obtaining the good BIOS image from the I/O firmware unit via the multi-port switch (Gentile, Fig. 1 #18, 19, 20, and paragraph [0013]).

As in claim 7, AAPA and Gentile disclose the multi-node computer comprises multiple nodes (AAPA specification, page 2 line 29 through page 3 line 2);

each node comprises at least one copy of the BIOS image in a central processing unit (CPU) firmware unit and at least one additional copy of the BIOS image in an input/output (I/O) firmware unit (AAPA specification, page 3 lines 2-3. Gentile discloses a computer system and a BIOS recovery server, each containing a copy of the BIOS image: computer system BIOS image: Fig. 1 #11; paragraph [0010] lines 7-9; BIOS recovery system BIOS image: Fig. 1 #19; paragraph [0013] lines 4-5);

each node further comprises a set of one or more CPUs (AAPA specification, page 3 lines 2-3);

each node further comprises a CPU hub interposed between the CPU firmware unit and the set of one or more CPUs (AAPA specification, page 3 lines 3-10);

each node further comprises a multi-port switch for internodal communication and an I/O hub interposed in series between the CPU hub and the I/O firmware unit (AAPA: specification, page 3 lines 3-10, Fig. 1; *EE TIMES* paragraph 7; *The Register* paragraph 6);

checking the CPU firmware units and the I/O firmware units to determine if any of the nodes contain a good copy of the BIOS image (Gentile, Fig. 1 #11 paragraph [0010] lines 6-8 disclose checking of corrupt BIOS);

and in response to determining that at least one of the nodes contains the good copy of the BIOS image, automatically copying the good copy of the BIOS image to all nodes that contain corrupted copies of the BIOS image (Gentile, Fig. 1 #18, 19 and 20, and described in paragraph [0013]).

As in claim 10, AAPA and Gentile disclose the MCS comprises multiple nodes, with each node containing a copy of the BIOS code (AAPA specification, page 2 line 29 through page 3 line 2; Gentile discloses a computer system and a BIOS recovery server, each containing a copy of the BIOS image: computer system BIOS image: Fig. 1 #11; paragraph [0010] lines 7-9; BIOS recovery system BIOS image: Fig. 1 #19; paragraph [0013] lines 4-5);

the BIOS recovery logic determines if any of the nodes contain a good copy of the BIOS code (Gentile, "validity check" depicted in Fig. 1 and described in paragraph [0010] lines 7-11);

and in response to determining that at least one node contains the good copy of the BIOS code, the BIOS recovery logic automatically causes the good copy of the BIOS code to be copied to any nodes that contain a corrupted copy of the BIOS code (Gentile, Fig. 1 #18, 19 and 20, and described in paragraph [0013]).

As in claim 11, AAPA and Gentile disclose a first CPU hub in the first node communicatively interposed between the first firmware unit and the first set of one or more CPUs (AAPA specification, page 3 lines 3-9);

a second CPU hub in the second node communicatively interposed between the second firmware unit and the second set of one or more CPUs (AAPA specification, page 3 lines 3-9);

a multi-port switch for internodal communications communicatively connected to the first CPU hub and the second CPU hub (AAPA specification, page 3 lines 6-10);

the BIOS recovery logic configures the multi-port switch to provide a communication path between the first CPU hub and the second CPU hub (AAPA specification, page 3 lines 6-10; Gentile, Fig. 2, paragraph [0010] lines 2-3, paragraph [0012] lines 2-4, where it is inherent there be a multi-node connection between the CPU and the other components present in the "computer system" and "BIOS recovery" system (read "CPU hub"). It is also inherent that there be a multi-port switch present in a WAN/LAN configuration in order to facilitate communication and transfer of information between the "computer system" and the "BIOS recovery system.");

and the BIOS recovery logic causes copies the good BIOS code from the second node to the first node via the multi-port switch (Gentile, Fig. 1, paragraph [0012] lines 1-5, paragraph [0013] lines 1-7, where it is inherent that "computer system" downloads a copy of the uncorrupted BIOS from the "BIOS recovery server.").

As in claim 12, AAPA and Gentile disclose the first and second firmware units comprise first and second central processing unit (CPU) firmware units

(AAPA specification, page 2 line 29 through page 3 line 2. Gentile discloses a "computer system" and a "BIOS recovery server" – computer system BIOS image: Fig. 1 #11; paragraph [0010] lines 7-9; BIOS recovery system BIOS image: Fig. 1 #19; paragraph [0013] lines 4-5 – which inherently comprise of CPU firmware);

the MCS further comprises an input/output (I/O) firmware unit communicatively connected to at least one of the first and second CPU firmware units (it would have been obvious to one skilled in the art at the time of the invention to connect I/O firmware housing the BIOS to at least one CPU firmware unit in order for the BIOS recovery system to properly occur as disclosed in Gentile in paragraph [0011] lines 3-8 and paragraph [0013]);

the I/O firmware unit also contains the BIOS code (by nature of the Basic Input/Output System, any combination of hardware and software specifically relating to the storage and functionality of the BIOS would be considered as "I/O firmware." Gentile, paragraph [0010] lines 7-9);

and in response to detecting corruption of the BIOS code in the first CPU firmware unit, the BIOS recovery logic automatically causes the BIOS code to be copied from the I/O firmware unit to the first CPU firmware unit (Gentile, paragraph [0011] lines 3-5 disclose detection of corrupt BIOS; paragraph [0013] lines 4-7 disclose automatic programming from the "I/O firmware" into the "CPU firmware unit" upon system reboot, where one skilled in the art would understand that BIOS code gets "programmed" into "CPU firmware" upon initialization of the system itself.)

As in claim 13, AAPA and Gentile disclose the first node comprises a first CPU hub communicatively connected to the first CPU firmware unit (AAPA specification, page 3 lines 2-4, where it is inherent that a "CPU hub" be connected to a "CPU firmware unit");

the second node comprises a second CPU hub communicatively connected to the second CPU firmware unit (AAPA specification, page 3 lines 2-4, where it is inherent that a second "CPU hub" would be connected to a second "CPU firmware unit" in the "four node-system" disclosed);

the MCS further comprises a multi-port switch for internodal communications communicatively interposed between the first CPU hub and the I/O firmware unit (AAPA: specification, page 3 lines 6-10; *EE TIMES* paragraph 7; *The Register* paragraph 6);

and the BIOS recovery logic causes the BIOS code to be copied from the I/O firmware unit via the multi-port switch (Gentile, paragraph [0006] lines 2-6 and Fig. 1 #19 and 20).

As in claim 14, AAPA and Gentile disclose the MCS further comprises an I/O hub communicatively interposed between the multi-port switch and the I/O firmware unit (AAPA: specification, page 3 lines 2-4, where one skilled in the art at the time of the invention would understand it necessary to have an "I/O hub" between an "I/O firmware unit" and any other device in order to allow for

communication with the other device or devices; *EE TIMES* paragraph 7; *The Register* paragraph 6);

and the BIOS recovery logic causes the BIOS code to be copies from the I/O firmware unit via the I/O hub (Gentile, paragraph [0006] lines 2-6 and Fig. 1 #19 and 20).

As in claim 15, AAPA and Gentile disclose the MCS comprises multiple nodes (AAPA specification, page 3 line 2);

each node comprises a set of one or more CPUs (AAPA specification, page 3 line 2-4);

each node further comprises a CPU firmware unit communicatively connected to the set of one or more CPUs (AAPA page 3 lines 2-10);

each node further comprises a CPU hub interposed between the CPU firmware unit and the set of one or more CPUs (AAPA specification, page 3 lines 2-5, Fig. 1 "SNC");

each node further comprises an input/output (I/O) firmware unit communicatively connected to the CPU hub (by nature of the Basic Input/Output System, any combination of hardware and software specifically relating to the storage and functionality of the BIOS would be considered as "I/O firmware." Gentile, paragraph [0010] lines 7-9, and paragraph [0011] lines 6-8);

each node further comprises at least one copy of the BIOS code the CPU firmware unit and at least one copy of the BIOS code in the I/O firmware unit (Gentile, paragraph [0010] lines 7-9, where it is inherent BIOS code be present in

the I/O firmware unit as described in the previous paragraph, and in the CPU in order to initialize the "computer system");

each node further comprises a multi-port switch for internodal communication and an I/O hub interposed in series between the CPU hub and the I/O firmware unit (AAPA: specification, page 3 lines 6-10; *EE TIMES* paragraph 7; *The Register* paragraph 6);

the BIOS recovery logic checks the CPU firmware units and the I/O firmware units to determine if any of the nodes contain a good copy of the BIOS code (Gentile, Fig. 1 #11 paragraph [0010] lines 6-8 disclose checking of corrupt BIOS, paragraph [0006] lines 2-5);

and in response to determining that at least one of the nodes contains the good copy of the BIOS code, the BIOS recovery logic automatically causes the good copy of the BIOS code to be copied to all nodes that contain corrupted copies of the BIOS code (Gentile, Fig. 1 #18, 19 and 20, and described in paragraph [0013]).

As in claim 17, AAPA and Gentile disclose the MCS comprises multiple nodes, with each node containing a copy of the BIOS image (AAPA specification, page 3 line 2; Gentile discloses a "computer system" BIOS image: Fig. 1 #11; paragraph [0010] lines 7-9 and a "BIOS recovery system" BIOS image: Fig. 1 #19; paragraph [0013] lines 4-5);

determining if any of the nodes contain a good copy of the BIOS image (Gentile, Fig. 1, paragraph [0010] lines 4-11);

and in response to determining that at least one node contains the good copy of the BIOS image, automatically copying the good copy of the BIOS image to any nodes that contain a corrupted copy of the BIOS image (Gentile, Fig. 1, paragraph [0006] and paragraph [0013]).

As in claim 18, AAPA and Gentile disclose the first node includes a first central processing unit (CPU) hub, the second node includes a second CPU hub, and the MCS further comprises a multi-port switch for internodal communications (AAPA: specification, page 3 lines 6-10; *EE TIMES* paragraph 7; *The Register* paragraph 6);

the operations performed by the recovery instructions further comprise configuring the multi-port switch to provide a communication path between the first CPU hub and the second CPU hub (AAPA specification page 3 line 10);

and the operation of automatically recovering from the corruption of the BIOS image comprises copying the good BIOS image from the second node to the first node via the multi-port switch (Gentile, Fig. 1, paragraph [0006] and paragraph [0013]).

As in claim 19, AAPA and Gentile disclose the first firmware unit comprises a central processing unit (CPU) firmware unit (AAPA specification, page 2 line 29 through page 3 line 2. Gentile discloses a "computer system" paragraph [0011], which inherently comprises of a CPU firmware unit);

the MCS further comprises an input/output (I/O) firmware unit (by nature of the Basic Input/Output System, any combination of hardware and software specifically relating to the storage and functionality of the BIOS would be considered as "I/O firmware." Gentile, paragraph [0010] lines 7-9, and paragraph [0011] lines 6-8);

in response to detecting corruption of the BIOS image in the CPU firmware unit, automatically causing a good BIOS image from the I/O firmware unit to be copied to the CPU firmware unit (Gentile, paragraph [0011] lines 3-5 disclose detection of corrupt BIOS; paragraph [0013] lines 4-7 disclose automatic programming into the "I/O firmware" into the "CPU firmware unit" upon system reboot, where one skilled in the art would understand that BIOS code gets "programmed" into "CPU firmware" upon initialization of the system itself.).

* * *

Claim 6 rejected under U.S.C. 103(a) as being unpatentable over Gentile, in view of AAPA, in further view of Goodman (U.S. PGPub 2002/0091807 A1).

Gentile and AAPA disclose the methods of claims 1 and 4 and the multi-node computer comprising of a first and second node (AAPA specification, page 2 line 29 through page 3 line 2). However, Gentile and AAPA do not teach replacing of more than one "bad" BIOS image. Goodman discloses a method which further comprises automatically using a good BIOS image in an I/O firmware unit in the second node to replace first and second bad BIOS images in

the CPU firmware units in the first and second nodes, respectively (Fig. 1 and 3, paragraphs [0021], [0027], and [0029]).

It would have been obvious to a person skilled in the art at the time of the invention to include recovering of a BIOS image in a system described by AAPA and Gentile where there is multiple BIOS firmware present using the method disclosed by Goodman. A person skilled in the art would have understood that Goodman's disclosure is appropriate for updating BIOS firmware in a multi-node computer because Goodman specifies updating of firmware versions (paragraph [0021] line 3) for use on EEPROM (paragraph [0019] line 8) memory automatically (paragraph [0021] lines 19-20) in a multi-nodal system similar to AAPA.

Claims 8 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Gentile, in view of AAPA, in further view of Fish et al. (U.S. PGPub 2002/0073353 A1).

Gentile and AAPA disclose the method of claim 1. However, Gentile and AAPA do not teach logging recovery information for future reference. Fish et al. disclose a method and apparatus for logging BIOS recovery information (Fig. 2 #216, abstract, paragraphs [0019] and [0025]).

It would have been obvious to a person skilled in the art at the time of the invention to include error logging of a BIOS recovery event. A person skilled in the art would have understood that it is important to retrieve error information

during a BIOS recovery execution in any type of computer system regardless of the number of "nodes" or physical scale of the computer system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (703) 605-4316. The examiner can normally be reached on Monday-Friday 7:30 am - 5:00 pm, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
August 17, 2004

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100